

## **REMARKS**

Claims 1-44 are currently pending in this application. Claims 1 and 44 have been amended. No new matter has been introduced. Claims 1, 40, 41, 42 43 and 44 are independent claims. Support for amendments made herein may be found, for example, in FIG. 1 and the corresponding discussion in Applicants' Specification.

### **WITHDRAWAL OF PREVIOUS REJECTIONS**

Applicants acknowledge the Examiner's withdrawal of the previous rejections under 35 U.S.C. § 112 and under 35 U.S.C. § 102(e) in view of U.S. Patent Application Publication No. 2004/0137745 ("*Houghton*").

### **35 U.S.C. §102(B) KOSHIISHI REJECTION**

The Examiner rejects claims 1, 2, 7, 12-13 and 44 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 5,919,332 ("*Koshiishi*"). Applicants respectfully traverse this rejection.

The Examiner asserts that Figure 1 of *Koshiishi* illustrates a bottom electrode 6, which acts as a stage, a solid upper electrode 21, an insulating member 31 arranged adjacent to the solid plate upper electrode 21. The Examiner asserts that there is a gap between insulating member 31 and the solid plate upper electrode 21 and asserts the gap is formed at the junction of the upper electrode 21 and the insulating plate 31.

Claim 1 requires, *inter alia*, an "insulating plate being configured such that only an edge portion of the outer electrode is exposed to the

bottom electrode." In *Koshiishi*, however, the insulating member 31 is arranged to, "cover the outer circumferential lower edge of the upper electrode 21," (See, *e.g.*, *Koshiishi* at 10:29 – 10:31) and insulate the upper electrode 21 and the processing container 3 (*Id.* at 10:25 – 10:28). In *Koshiishi*, the entire surface of the upper electrode 21 is exposed to the bottom electrode 6. Consequently, *Koshiishi* differs from the apparatus of claim 1 in that the insulating member 31 of *Koshiishi* is not "configured such that only an edge portion of the outer electrode is exposed to the bottom electrode." For at least this reason, claim 1 is patentable over *Koshiishi*. Claims 2, 7, 12 and 13 are patentable over *Koshiishi* at least by virtue of their dependency from claim 1.

Furthermore, claim 44 is directed to an insulating plate, "shaped so as to guide gas away from a center portion of a semiconductor wafer." *Koshiishi* fails to teach or suggest such an insulating plate. As discussed above, the insulating member 31 of *Koshiishi* is arranged to "cover the outer circumferential lower edge of the upper electrode 21," (See, *e.g.*, *Koshiishi* at 10:29 – 10:31) and insulate the upper electrode 21 and the processing container 3 (*Id.* at 10:25 – 10:28). *Koshiishi* does not, however, disclose that the shape of the insulating member 31 guides gas away from a center portion of the wafer W in any way. Consequently, claim 44 is believed to be patentable over *Koshiishi*.

### **35 U.S.C. § 102(b) Fujimoto Rejection**

The Examiner also rejects of claims 1-2, 7, 12-13 and 44 under 35 U.S.C. §102(b) as anticipated by U.S. Patent 5,413,673 ("*Fujimoto*").

Applicants respectfully traverse this rejection.

The Examiner asserts that Figures 4 and 5 of *Fujimoto* illustrates a bottom electrode 52, which acts as a stage for semiconductor wafer 50, an upper electrode 51 arranged above the semiconductor wafer, and dielectric spacers 42 arranged adjacent to the upper electrode 51 with a gap there between.

As set forth above with respect to *Koshiishi*, however, the dielectric spacers 42 of *Fujimoto* are not, "configured such that only an edge portion of the outer electrode is exposed to the bottom electrode," as is the case with the insulating plate of claim 1. To the contrary, as is evident from FIG. 4 of *Fujimoto*, for example, a central portion of the upper electrode 51 is always exposed to the bottom electrode 52. For at least this reason, claim 1 is patentable over *Fujimoto*. Claims 2, 7 and 12-13 are patentable over *Fujimoto* at least by virtue of their dependency from claim 1.

Furthermore, as also discussed above, claim 44 is directed to an insulating plate "shaped so as to guide gas away from a center portion of a semiconductor wafer." *Fujimoto* fails to teach or suggest such an insulating plate. As is evident from FIG. 5B, in the least, the dielectric spacers 42 are arranged so as to guide gas towards the central portion of

the wafer 50. Consequently, claim 44 is believed to be patentable over *Fujimoto*.

### **35 U.S.C. §102(b) Quon Rejection**

The Examiner also rejects claims 1-8, 19-21, 30 and 31 under 35 U.S.C. § 102(e) as anticipated by U.S. Patent Application Publication No. 2003/0150562 ("*Quon*"). Applicants respectfully traverse this rejection.

The Examiner asserts that *Quon* discloses a bottom electrode 20 below a semiconductor wafer 14 which acts as a stage. The Examiner further asserts that *Quon* teaches an upper electrode 10 arranged above the semiconductor wafer and a ceramic washer (insulator) 80 arranged adjacent to the solid upper plate electrode 10.

As set forth above with respect to *Koshiishi*, however, the ceramic washer 80 of *Quon* is not, "configured such that only an edge portion of the outer electrode is exposed to the bottom electrode," as is the case with the insulating plate of claim 1. As is evident from FIG. 1 of *Quon*, the entire surface of the upper electrode 10 is exposed to the bottom electrode 20. Therefore, the ceramic washer 80 of *Quon* does not constitute the "insulating plate," of claim 1. For at least this reason, claim 1 is patentable over *Quon*. Claims 2-8, 19-21, 30 and 31 are patentable over *Quon* at least by virtue of their dependency from claim 1.

### **35 U.S.C. § 102(e) Kim Rejection**

The Examiner also rejects claims 1-2, 7 and 12 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Publication 2003/0070760 ("*Kim*"). Applicants respectfully traverse this rejection.

The Examiner asserts that *Kim* teaches a bottom electrode 155 arranged below a semiconductor wafer 154 acting as a stage, a solid upper electrode 151 arranged above the semiconductor wafer 154 and an dielectric body (insulator) 152 arranged adjacent to the solid plate upper electrode 151 with a gap 153 there between.

As set forth above with respect to *Koshiishi et al*, the dielectric body 152 of *Kim* is not, "configured such that only an edge portion of the outer electrode is exposed to the bottom electrode," as is the case with the insulating plate of claim 1. As is evident from FIG. 2B of *Kim*, for example, multiple center portions of the upper electrode 151 are exposed to the bottom electrode 155 through capillaries 153. Therefore, the dielectric body 152 of *Kim* does not constitute the "insulating plate," of claim 1. For at least this reason, claim 1 is patentable over *Kim*. Claims 2, 7 and 12 are patentable over *Kim* at least by virtue of their dependency from claim 1.

### **35 U.S.C. § 102(e) Berman Rejections**

Claim 44 stands rejected under 35 U.S.C §102(e) as being anticipated by U.S. Patent 6,837,967 ("*Berman*"). This rejection is respectfully traversed.

The Examiner refers to the entirety of *Berman* to allegedly teach the "insulating plate," of claim 44. In particular, however, the Examiner directs Applicants attention to FIGS. 2A-2D of *Berman*. Contrary to the Examiner's assertion, FIGS. 2A-2D of *Berman* illustrate top views of a

mounted wafer, but not an insulating plate. In fact, no portion of *Berman* teaches or suggests the "insulating plate," of claim 44. For at least this reason, claim 44 is patentable over *Berman*.

### **35 U.S.C. § 103 REJECTIONS**

Under 35 U.S.C. § 103, claim 9 stands rejected as unpatentable over *Quon* in view of U.S. Patent Application Publication No. 2003/0201069 ("*Johnson*"); claims 1-8, 10, 11, 17-22, 28-32, 38 and 39 stand rejected as unpatentable over *Houghton* in view of *Quon*; claim 9 stands rejected as unpatentable over *Houghton*, *Quon*, and further in view of *Johnson*; and claims 12-16, 23-27 and 33-37 stand rejected as unpatentable over *Houghton* in view of *Quon* and further in view of *Koshiishi*. Applicants respectfully assert that each of these rejections has been overcome by overcoming the various rejections of independent claim 1. Accordingly, reconsideration of this rejection and allowance of each of these dependent claims is respectfully requested.

### **CONCLUSION**

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of the pending claims in connection with the present application is earnestly solicited.

If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number listed below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY & PIERCE, PLC

By



John A. Castellano  
Reg. No. 35,094

JAC/AMW:krm

AW

P.O. Box 8910  
Reston, VA 20195  
(703) 668-8000